Reconfigurable RF Systems Using Commercially Available Digital Capacitor Arrays

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Abstract: *Various RF circuit blocks implemented by using commercially available MEMS digital capacitor arrays are presented for reconfigurable RF systems. The designed circuit blocks are impedance-matching network, tunable bandpass filter, and VSWR sensor. The frequency range of the designed circuits is 0.4-4GHz. The MEMS digital capacitor arrays that are employed in the designs have built-in dc-to-dc voltage converter and serial interface significantly simplifying the control circuitry. The RF circuit blocks are suitable to low-cost, high-level of integration, thanks to the commercially available parts and standard RF packaging technologies.*

Keywords: Reconfigurable RF System; Tunable RF Filter; Tunable Impedance Matching Network; VSWR Sensor; MEMS; Digital Capacitor Array.

Introduction

Traditionally, RF systems have been designed and built under strict assumptions such as the source impedance, load impedance, and frequency bandwidth. Adapting an RF system to changing impedance levels and frequency bands without affecting the efficiency, noise figure, and other critical system parameters has been one of the significant challenges in multi-band, compact RF systems. This is not a trivial task due to the distributed nature of RF signals and parasitic effects that become more important at higher frequencies. The resulting complex interactions between the components at RF frequencies and efficiency degradation due to RF losses make the dynamic tuning of RF systems challenging.

In our work on the DARPA RF-FPGA program, we will address this issue by dividing the problem in two parts. In the first part, we will use a wideband "RF engine" built from radio frequency integrated circuit (RFIC) technology. In a RFIC design, dimensions of the passive components can be assumed lumped from RF signal point of view. Therefore, traditional analog design techniques can be employed to achieve broad-band operation and reconfigurability provided that RF transistors with high transition frequencies are used. However, this approach has a drawback: the quality factor of the on-chip passive circuits also drops as the size reduces due to higher RF insertion losses. This is a serious limitation in designing, for instance, tunable filters for channel selection or impedance matching networks for high-efficiency power amplifiers where low-loss is a critical performance parameter. To alleviate this problem, the second part of our solution is to utilize a tunable front-end module that utilizes high-Q off-chip passive components to obtain a better performance.

Canonical block diagrams for reconfigurable RF transmitter and receiver utilizing the above mentioned approach is presented in Figure 1. The wideband RF engine shown in the transmit block diagram accepts complex baseband data and commands for the center frequency, baseband bandwidth, modulation type, etc., and generates the specified waveform. The RF engine output passes through the tunable front-end module (FEM) where it receives filtering, amplification, and impedance adjustment. The adjustable sub-blocks in the FEM are tuned to the desired center frequency. In addition, there is a wideband VSWR sensor to permit adaptable impedance matching network for changing antenna loading. Note that for the receiver circuitry, the path through the FEM is reversed and the wideband RF engine is given appropriate commands to produce baseband, complex data as an output.

Our goal in the RF-FPGA program is to construct RF modules that can be tuned over the 0.4–4 GHz band, providing optimized RF performance through high-level commands that set the center frequency, bandwidth and few other parameters of interest to the signal designer. Some of the salient features of such an approach are listed below:

- It removes the detailed RF design from the end user by providing programmable components to meet the system-level needs,

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14. ABSTRACT
Various RF circuit blocks implemented by using commercially available MEMS digital capacitor arrays are presented for reconfigurable RF systems. The designed circuit blocks are impedance-matching network, tunable bandpass filter, and VSWR sensor. The frequency range of the designed circuits is 0.4-4GHz. The MEMS digital capacitor arrays that are employed in the designs have built-in dc-to-dc voltage converter and serial interface significantly simplifying the control circuitry. The RF circuit blocks are suitable to low-cost, high-level of integration, thanks to the commercially available parts and standard RF packaging technologies.

15. SUBJECT TERMS

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- It allows the RF functionality to be produced in large volumes, thereby bringing down the cost of these components,
- It permits field upgrades of the system such as changes in center frequency and/or bandwidth, and,
- It provides a mechanism for real-time adaptable systems RF systems when paired with appropriate control logic.

Advanced RF plastic packaging and PCB design technologies allow flip-chip attachment of RFICs on various types of substrates providing a pathway to such implementation. Conceptual cross-section of the programmable RF front-end system using commercial tunable elements and packaging technology is shown in Figure 2.

In this paper, we will present designs of three types of tunable RF blocks that can be used in the reconfigurable RF systems as described above: tunable impedance-matching network, tunable RF filter, and VSWR sensor. The designs are based on commercially available parts to achieve a low-cost and easy implementation.

Tunable Impedance-Matching Network

A tunable impedance-matching network is commonly used to match variable antenna impedance to the transmitter output or receiver input [1, 2]. There are multiple utilities for this device. In one, the so-called static mode, the antenna can be matched to the rest of the system before the system is deployed to overcome variations in the manufacturing process, say of a narrow band antenna. In a second, the so-called dynamic mode, the impedance changes are compensated in real-time based on the output from the VSWR sensor and can be used to overcome variation in the antenna impedance caused by changes in external loading.

A typical topology for a tunable impedance-matching network is shown in Figure 3. All tunable capacitors shown in the figure are implemented using wiSpry WS1033 digital capacitor array, which is a commercially available part. The impedance-matching network is controlled via a serial interface using a microcontroller. Manufactured prototype of the matching network is shown in Figure 4. Since it must be used in the direct RF path, the insertion loss of the matching network is a paramount consideration. In order to achieve a good quality factor with repeatable performance, all inductors are implemented using microstrip lines. Usage of microstrip lines also enables better control on the parasitics via full-wave EM simulations of the circuit layout (except the tunable capacitors). Another important consideration is the parasitic components of the digital capacitor array. The packaged WS1033 chip has certain amount of parasitic capacitances presented at the RF terminals. This has a detrimental effect on the frequency coverage. Therefore, the matching network has to be optimized accordingly.

Tunable RF Bandpass Filter

A tunable bandpass filter is a narrow bandpass filter where the center frequency can be adjusted in a given frequency band [3, 4]. The filter can be used in both transmit and receive paths. In the transmit path, it rejects undesired spurious signals keeping the transmitted spectrum clean, and in the receive path, it ensures low noise floor and reduces saturation effects due to high-level interference signals.

The filter topology employed in this work is shown in Figure 5. The center frequency is adjusted by changing C_T. The purpose of C_M is to match the filter to load and source impedance as the resonator impedance changes. All tunable capacitors shown in the figure are implemented using wiSpry WS1033 digital capacitor array. The coupled inductors shown in the figure is implemented using microstrip lines. Manufactured prototype of the matching network is shown in Figure 6. The center frequency of the filter is controlled via a serial interface using a microcontroller. As in design of the tunable impedance-matching network, the parasitic capacitances of the WS1033 digital capacitor array limit the tuning range of the filter.

As an example, simulated frequency responses of the filter are given in Figure 7 and 8 for two different coupled microstrip line lengths.

VSWR Sensor

The purpose of a VSWR sensor is to extract the complex reflection coefficient of the load (e.g., the antenna). Using this information, the system can tune the impedance-matching network more efficiently and quickly so that the transmitter and receiver are always matched to antenna for optimum performance. There are different methods of implementing VSWR sensors in the literature [5, 6, 7]. Probably the most straightforward and traditional way of achieving this functionality is to use directional couplers to separate the forward and backward traveling ways. However, the directional coupler networks are bulky

at lower frequencies and not suitable for high-level of integration. One alternative technique is to sample the RF voltage and current waveforms directly using a sense transformer. Then, one can determine the load impedance from the vector values of current and voltage. However, the high insertion-loss of the sense transformer limits the usability of this approach in the direct RF path of the transceiver. Besides, the sense-transformer limits the upper usable frequency range.

An alternative way is to use a linear *N*-port and extract the complex load using the sampled RF voltages and Y-parameters of the *N*-port network. This approach is demonstrated in Figure 9. Provided that the *Y*-parameters of the *N*-port network are known to a sufficient degree of accuracy, this method provides the most flexible way of extracting the complex load impedance. Note that the *N*-port network approach does not suffer the limitations of the sense-transformer method; it can be made sufficiently low-loss and broadband so that it can be used on the main RF path without degrading the performance.

Conclusion

In this paper, we have presented various tunable RF blocks that will be used in the tunable front-end module of our approach to the RF-FPGA program. The presented RF blocks are tunable impedance-matching network, tunable bandpass filter, and VSWR sensor. Commercially available MEMS digital capacitor arrays have been used to implement the tuning functionality. The capacitor array chips have built-in dc-to-dc voltage converter and a serial interface tremendously simplifying the implementation. The use of commercially available parts provides a low-cost solution for the reconfigurable RF systems.

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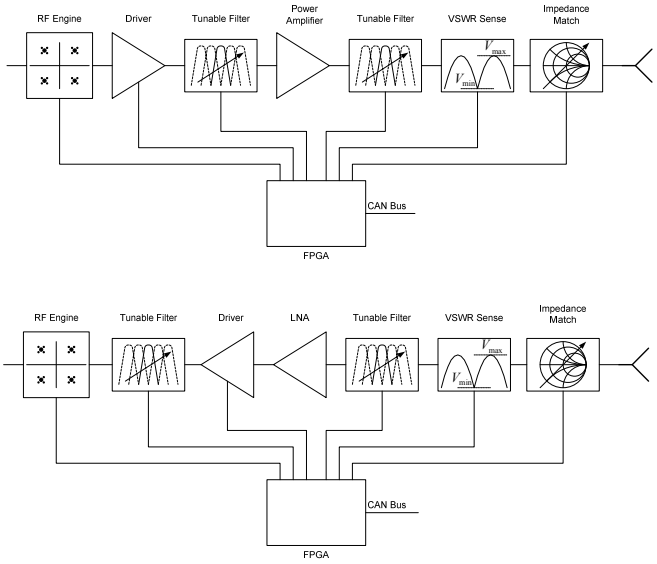

Figure 1: Block diagrams of configurable RF transmitter and receiver. Note that depending on the system requirements, tunable filter locations may be different.

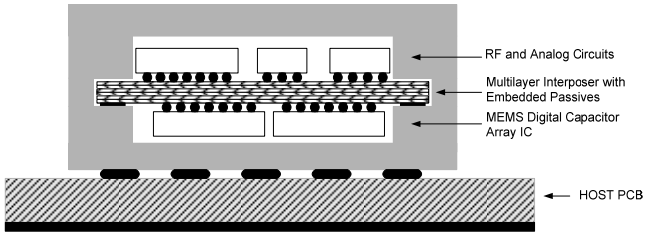

Figure 2: Conceptual cross-section of the programmable RF front-end system using commercial tunable elements and packaging technology.

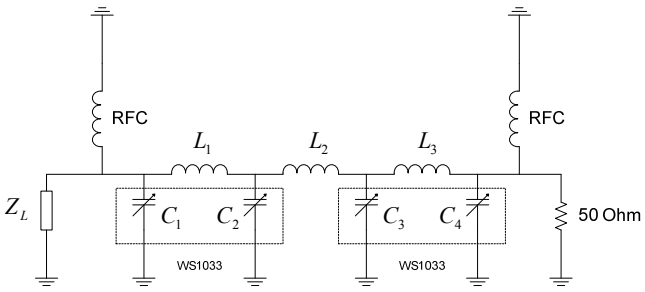

Figure 3: Equivalent circuit of the tunable impedance-matching network. The choke inductors are for ESD protection. All inductors are implemented using microstrip lines.

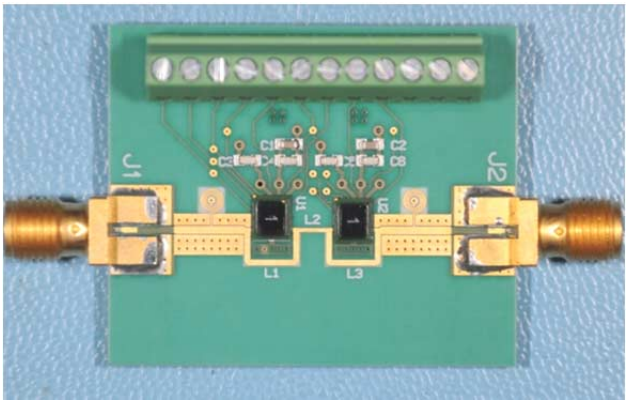

Figure 4: Photograph of the designed tunable impedance-matching network prototype PCB.

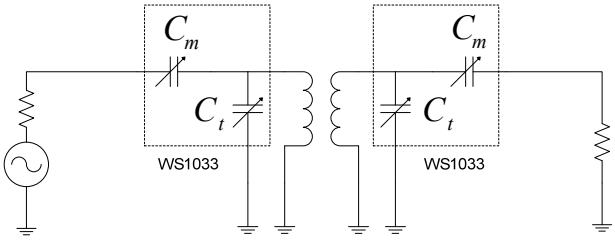

Figure 5: Equivalent circuit of the tunable bandpass filter network. The capacitors are used to tune the center frequency. The capacitors are used to adjust matching.

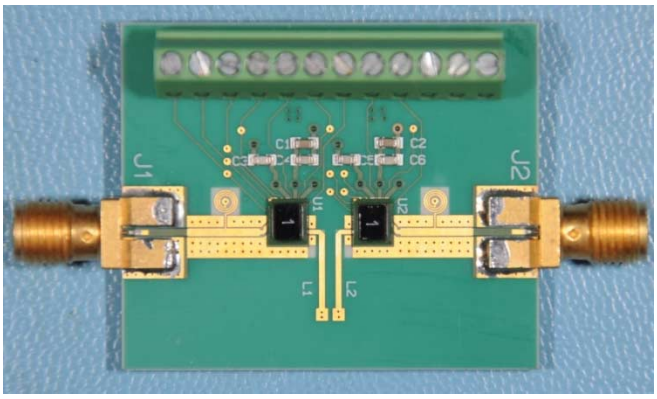

Figure 6: Photograph of the designed tunable bandpass network prototype PCB.

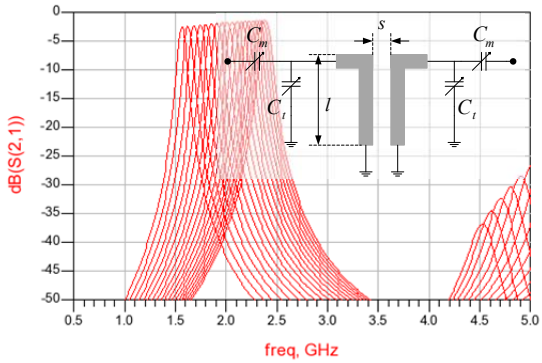

Figure 7: Simulation results of the tunable filter network. The inset figures show the actual layout of the coupled transformer and filter parameters (, ,).

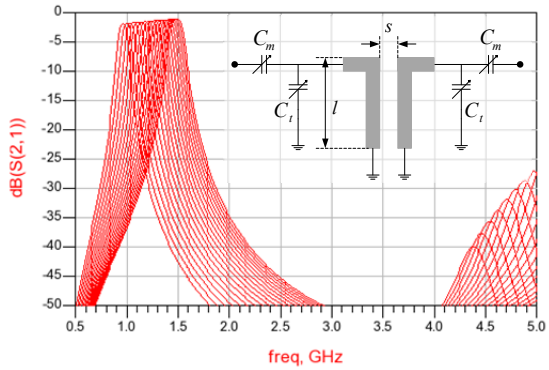

Figure 8: Simulation results of the tunable filter network. The inset figures show the actual layout of the coupled transformer and filter parameters (, , ,).

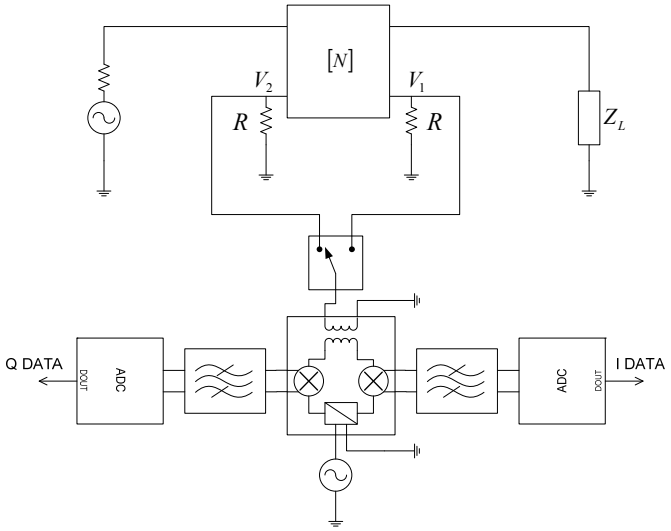

Figure 9: Block diagram of the VSWR sensor employing linear *N*-port network. By vector sampling the voltages on the network terminals and using *Y*-parameters of the linear network, one can extract the load impedance, .